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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,701	02/19/2004	Iwao Sugiura	042113	3201

38834 7590 01/05/2007

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,701	SUGIURA ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-19 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4, 5, 7-19, and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on October 11, 2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 7-9, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga (US 6,670,710 B2) in view of Vigna et al. (US 6,605,873 B1).

In re claim 1, Matsunaga shows (figs. 1-3) a semiconductor device comprising a substrate (11); a first multilayer interconnection structure (13, 14, 16, 18) formed on said substrate; and second multilayer interconnection structure (19, 22) formed on said first multilayer interconnection structure, said first multilayer interconnection structure including a first interlayer insulation film (13, 14, 16, 18) and a first interconnection layer (not label and next to layers 15, 17) included in said first interlayer insulation film; said second multilayer interconnection structure including a second interlayer insulation film (19, 22) and a second interconnection layer (not labeled and next to layers 20, 21) included in said second interlayer insulation film, said first multilayer interconnection structure including a pillar (30) extending from a surface of said substrate and reaching at least said second multilayer interconnection structure, said first interconnection layer

being formed so as to avoid said pillar. Matsunaga shows that there is an electrode pad area (35/36) formed above the substrate but does not specifically show the pillar being formed in a region of the substrate right underneath the electrode pad or the pillar being provided on a device isolation structure. Vigna shows (figs. 1-3) a semiconductor device in which a mechanical stress bearing structure (31) comprising pillar/via/plug portions (24, 19, and 12) is formed beneath an electrode pad (28). The mechanical stress bearing structure is formed on the a device isolation structure (field oxide regions 6) of the substrate. With this configuration, mechanical stress exerted during a wire bonding process is distributed to the peripheral areas of substrate and reduced on the active region components (3) (col. 3, lines 20-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pillar structure of Matsunaga by forming it on a device isolation structure and beneath an electrode pad as taught by Vigna to distribute stress from the device regions of the substrate to the device isolation regions during a wiring bonding process.

In re claim 2, Matsunaga shows (figs. 1-3) that said pillar has a layered structure identical to a layered structure of said first interconnection layer in said first multilayer interconnection structure.

In re claim 4, Matsunaga shows (figs. 1-3) that said pillar has an edge part engaging to a bottom surface (17) of said second multilayer interconnection structure.

In re claim 5, Matsunaga shows (figs. 1-3) that said pillar extends further in said second multilayer interconnection structure and has a layered structure identical to a

layered structure of said second interconnection layer in a part thereof extending in said second multilayer interconnection structure.

In re claim 7, Matsunaga shows (figs. 1-3) an electrode pad (46) is formed on said second multilayer interconnection structure.

In re claim 8, the references do not specifically disclose that the plural numbers of pillars occupy at least 15% of the area. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the pillars in a desired amount suitable for the electrode pad reinforcement, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 9, Matsunaga shows (figs. 1-3) that there is formed an active device (12) in region of said substrate right underneath said electrode pad.

In re claim 13, Matsunaga does not specifically disclose said pillar has a Young modulus of 30GPa or more. However, the pillar inherently has such a property since it has the same structure and materials as the instant invention.

In re claim 14, Matsunaga shows (figs. 1-3) that in said first multilayer interconnection structure, said pillar is formed with plural numbers so as to be located at both sides of an interconnection pattern forming a part of said first interconnection layer Figure 1, shows an overhead view in which the pillar (30) surrounds the devices region.

In re claims 15 and 16, Matsunaga shows (fig. 1) that said pillar (30) forms a wall extending continuously on said surface of said substrate. The pillar extends

continuously along a circumference of said substrate in said first and second multilayer interconnection structures and form a guard ring.

Claims 10-12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga (US 6,670,710 B2) in view of Vigna et al. (US 6,605,873 B1) as applied to claim 1 above, and further in view of the Applicant's Prior Art Figures 1-4 (APAF).

In re claims 10-12 and 17-19 concerning the first and second interlayer insulating films each having a desired Young's Modulus, Matsunaga and Vigna do not disclose those properties of the film. However, the APAF 1 shows that a first interlayer insulating film (14-17) and a second interlayer insulating film (18-21) each have the desired properties of the claimed invention in that the first film has Young's Modulus lower than the Young's Modulus of the second film. The specification on pages 7-12 lists all of the properties of the first interlayer insulating film of the porous organic film and the second interlayer insulating film of a CVD material. With such a configuration, the semiconductor device combined with the metallization structure has reduced signal delay and high speed operation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulation materials of Matsunaga and Vigna by using the low Young's Modulus first interlayer insulation film and the higher Young's Modulus second interlayer insulation film as taught by the APAF to form a device having reduced signal delay and high speed operation.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga (US 6,670,710 B2) in view of Vigna et al. (US 6,605,873 B1) as applied to claim 1 above, and further in view of Sugiyama et al. (US Pub. 2002/0040986 A1).

In re claim 20, Matsunaga and Vigna show all of the elements of the claims except said pillar is provided in plural number on said substrate, and wherein there is formed a reinforcement structure in said first multilayer interconnection structure so as to extend diagonally between said plural pillars. Sugiyama et al. shows (fig. 7) a more detailed interconnection layout in which the interconnect structure (104) is formed diagonally in the multilayered structure of layers 88, 90, and 92 and within the boundaries of the pillar structure (102 and 106). While Sugiyama only discloses this configuration to form a specific connection scheme in the interconnect structure, it is inherent that such a structure also provides reinforcement to the interlay insulation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the interconnect of Matsunaga and Vigna by forming the interconnects in a diagonal configuration as taught by Sugiyama to form a specific routing scheme.

Response to Arguments

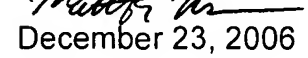
Applicant's arguments with respect to claims 1, 2, 4, 5, 7-19, and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren

December 23, 2006